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| 10/017,990 | 12/14/2001 | Xiaoju Wu | TI-31214 | 8404 |

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| EXAMINER | |
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| FARAHANI, DANA | |
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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Paper No. 13

Application Number: 10/017,990
Filing Date: December 14, 2001
Appellant(s): WU ET AL.

Peter McLarty
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 8/15/03.

***(1) Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

***(2) Related Appeals and Interferences***

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

***(3) Status of Claims***

The statement of the status of the claims contained in the brief is correct.

***(4) Status of Amendments After Final***

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

***(5) Summary of Invention***

The summary of invention contained in the brief is correct.

***(6) Issues***

The appellant's statement of the issues in the brief is correct.

***(7) Grouping of Claims***

The rejection of claims 1-30 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

***(8) Claims Appealed***

The copy of the appealed claims contained in the Appendix to the brief is correct.

***(9) Prior Art of Record***

| | | |
|---|---|---|
| 5,179,432 | HUSHER | 1-1993 |
| 5,399,510 | TANIGUCHI | 3-1995 |

S.M. Sze, Semiconductor Devices, Physics and Technology, 1985, John Wiley & Sons, 1st edition, page 139.

***(10) Grounds of Rejection***

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, 4-6, 8, 13, 15, 17, 21-24, 27, 29, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Husher.

Regarding claims 1, 8, 13, 15, 17, 21-24, 27, 29, and 30, Husher discloses in figure 3 an electronic circuit, comprising: a semiconductor substrate 100; a first layer 110 in a fixed physical relation to the semiconductor substrate; a well 160 formed in the first layer, wherein the well comprises a first conductivity type and has a side dimension

and a bottom dimension; a first enclosure 180, and 170, surrounding the side dimension and the bottom dimension of the well, wherein the first enclosure comprises a second conductivity type complementary of the first conductivity type and has a side dimension and a bottom dimension; and a second enclosure (190 and substrate 100) surrounding the side dimension and the bottom dimension of the first enclosure, wherein the second enclosure comprises the first conductivity type.

Regarding claim 2, layer 150 is a buried layer (see column 4, lines 53-56).

Regarding claim 4, layer 170 is adjacent layer 150.

Regarding claim 5, layer 110 is an epitaxial layer (see column 4, lines 53-60).

Regarding claim 6, see figure 3.

Claims 3, 7, 10, 14, 25, 26, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Husher, further in view of Taniguchi.

Regarding claims 3, 7, 10, 14, and 25, Husher discloses the claimed invention, as discussed above, except for the first conductivity type being n-type, and the second conductivity type being p-type. Taniguchi teaches at column 7, lines 5-9, that PNP and NPN transistors are equivalently produced in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to make the first conductivity type n-type, and the second conductivity type p-type in order to make a PNP bipolar transistor instead of an NPN bipolar transistor, since they are both used in the art according to a particular application.

Regarding claims 26 and 28, Husher discloses a dosage of 5 * 10^15 for buried layer 170 with an energy of 80 KeV (see column 4, lines 63-68).

Husher does not disclose an energy on the order of 60 KeV.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to lower the energy in order to adjust the ion implantation process with the existing ion implanting environment, that is temperature and time, and also, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 9, 11, 12, 16, 18, 19, and 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Husher as applied to claims 8 above, and further in view of Semiconductor Devices, Physics and Technology.

Husher renders the claimed invention obvious, as discussed above, except for a circuitry connecting the first terminal (first enclosure) to the second terminal (second enclosure).

Sze discloses on page 139, figure a, and the paragraph above the figure, a circuitry at the left hand side of the figure for connecting the base of a bipolar transistor to the emitter in order to obtain the switching characteristic of the transistor, shown below figure "a". The first enclosure and the second enclosure are emitter and base, respectively. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a circuitry to connect the base and emitter in order to obtain the switching characteristic of the bipolar transistor in Husher's invention.

***(11) Response to Argument***

Appellants argue that the examiner's description of region 160 of figure 3 of the Husher patent being a well is incorrect. In support of this assertion, appellants explain that region 160 is called an annular P+ sinker region (column 3, lines 67-68 of the reference), while claims 1 and 22 call for a well region. Moreover, it is stated in the Appeal Brief that the word well refers to a region that has a specific function and an "electronic device" is formed therein (see page 4, the last paragraph).

The examiner maintains that the word "well" in semiconductor terminology has a broader meaning than that as defined by the appellants. First, every region in a semiconductor device (or substrate) has a specific function, otherwise it wouldn't be in the device. Second, while an electronic device, or devices might be formed in a well region, this is not necessary. The word "well" is a broad term that could be any doped region in a semiconductor substrate. U.S. patent 5,828,124 to Villa is presented to support this statement. Villa, in figure 3, calls region 46' a well region (see column 3, line 62). Incidentally, region 46' is annular, and it is just a P doped region in the device, between the emitter E and base B. Region 48 of figure 2 is also called a well region (see column 3, line 50). Region 48 is yet another P doped region in the device. Therefore, calling region 160 of the Husher reference a "well" region is in line with what is commonly understood to be a well region in the art.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Dana Farahani
Examiner
Art Unit 2814

October 31, 2003

Conferees
Brian Sircus
Wael Fahmy

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